REMARKS

Claims 1-17 are pending in the application. Claims 1-17 are rejected under 35 U.S.C§102(e) as anticipated by Moriwaki et al. (US 6,507,584) (Moriwaki).

Overview of the Specification

The specification describes an invention where a packet switch device includes a buffer at the input stage of the packet switch, the packet switch includes a crossbar switch (an XB-SW).

A feature associated with an embodiment of applicant's invention lies in accomplishing high-speed switching without requiring a buffer provided to the crossbar switch and under a condition associated with a fixed delay time by causing a distribution unit to distribute arriving packets to a plurality of paths of the crossbar switch respectively in the order of these packets to arrive and a multiplexing unit to perform a process representing an inversion of the process performed by the distribution unit with respect to the packets which have been switched by the crossbar switch.

Claim 1

In the Office Action Fig. 1 and col. 6, lines 63-67 of Moriwaki are pointed to as anticipating applicant's features. In particular applicant's distribution unit is compared to the cell distributor 20-n of Moriwaki.

However col. 6, lines 63-67 describes the ATM cells read from cell buffer 23 by use of the RA 27. Col. 6, lines 47-62 describes:

"To generate the read address (RA) of the cell buffer 23, the output port information selected by the queue selector 243 is input into the RA generator 241. In the RA generator 241, the ATM cell read instructions for the queuing buffers 23-1 to 23-N are generated based on the number specified from distributive number register 244. More particular, the RA generator 241

generates RA 27 to read ATM cells from one of the queuing-buffers 23-1 to 23-N that corresponds to an output port based on the output of the queue selector 243." (Emphasis added).

"The value of the cell counter 242 for all output ports is input into queue selector 243 so that the queue selector 243 selects one of the output ports having the most ATM cells directed thereto." Col. 5, lines 43-46.

This is different from the claimed invention where: a distributing unit sequentially distributing input packets to a plurality of paths in an arrival order in units of packets."

Moriwaki is different from the claimed invention because Moriwaki reads from the queuing buffers based on the queue selector 243. In contrast applicant claims a distributing unit sequentially distributing input packets to a plurality of paths in an arrival order.

In summary Moriwaki only describes the distributors 20-n having a cell buffer 23 and distributing cells to ATM SW input ports in the order determined by RA and distributing the same destination packets to the same output line among the ATM switch ports 41-1 to 41-4 sequentially. In other words, RA collects packets of which the destinations are the same and instruct the cell buffer, after changing the order of packets for outputting them to the same destination packets at once.

Claim 2

Dependent claim 2 describes multiplexing packets associated with the plurality of input highways to the same port into fixed ordered slots. In the Office Action Fig. 4 and col. 6, lines 63-67 of Moriwaki are pointed to as anticipating applicant's features.

It is respectfully submitted that Moriwaki does not describe the features of claim 1 and in addition fails to described the fixed ordered slots because Moriwaki describes "[T]he cell

distributor 22 adjusts a timing of output cells, each of which have the same destination information." (emphasis added, col. 6, lines 66-67).

It is submitted that Fig. 4 and col. 6, lines 63-67 in Moriwaki et al. are, as reviewed above, only concerned with assembling respective input highway cells based on associated destinations as instructed by RA 27 and multiplexing those associated with the same destination by 27.

Claim 3

Claim 3 includes the features of claim 1 and in addition includes a configuration in which the switch is, further logically divided into a plurality of switch planes and operated on a same one circuit, in which the number of switch planes is set to be correspondent to the capacity of the switch.

Claim 4

Claim 4 describes the packet switch device of claim 1 and further provided with highway interfaces (HW-Ifs) associated with respectively different numbers of accommodation lines and in particular, the number of switch units are made to match numbers required by a distributing unit and multiplexing unit, which have a maximum number of accommodated lines.

Moriwaki describes in Col. 3, lines 15-35 and col. 5, lines 30-35 assembling all the same destination ATM cells based on routing information held in each header and consequently it becomes possible to expand an ATM switch.

However this is different from the claimed invention in which by equating all the highway interfaces to that associated with the largest number of accommodation lines and providing the same number of input lines to all the switches for equating switching operations of all the switches.

Claims 5, 10, 13 and 17

Claims 5, 10, 13 and 17 are amended to clarify that the configuration in accordance with claims 1 and 4 and are further associated with assigning a fixed offset to tags of input highways sequentially, in a manner in which the lengths (values) of these offset vary sequentially between those associated with different input-highway tags. This amendment is supported, for example, by Fig. 7 and the Fig. 7 related description found in lines between line 21 on page 17 and line 5 on page 8. In addition to the further description relating back to Fig. 5.

In the Office Action Fig. 4, controller 24 and distributive number register 244 in which the read number of the cell buffer 23 is stored are Moriwaki pointed to as anticipating applicant's features.

Applicant's claim 5 is concerned with adding a fixed length offset to the output highway information contained in each of the tags of input packets sequentially in which the offset time lengths added to those of the same input highway packets are set to be the same but different from the offset time lengths added to different input highway packets (a same fixed offset time length is added to those associated with the same input ports of the switch), performing switching processes with respect to packets after these offset adding processes and outputting cells of a plurality of highways from one port.

As a result of this configuration, one circuit becomes enough for operating all the switches, and hence it becomes possible to compose both the switching unit and converting unit by one switching circuit. Moriwaki et al. does not teach this feature at all. Fig. 4 of Moriwaki et al. is concerned only with an initial value held in the distribution number register 244 is controlled by RA based on header information and Fig. 9 of Moriwaki et al. is concerned only with a multiplexing process associated with a multiplexer.

Claim 10, 13 and 17, although different in scope from claim 5, also includes the distinguishing features discussed above.

Claims 6, 7, 8 and 9

Applicant's claim 6 includes the features of claim 1 and in addtion includes a unique combination of features which are not described nor suggested in the cited reference. The office action points to the scalability of the ATM switch in the reference. However the reference fails to describe: When said switch unit is expanded, said distributing unit, said multiplexing unit, and said switch unit are expanded, and operations of said distributing unit, said multiplexing unit, and said switch unit are changed after a packet output of said input buffer unit is once suspended, and the packet output of said input buffer unit is resumed, so that the switch unit can be expanded online.

Claims 7-9 depend from claim 6 and include additional distinguishing features

Claim 11

Applicant claims sequentially distributing input packets to a plurality of paths in an arrival order in units of packets.

In Moriwaki the value of the cell counter 242 for all output ports is input into queue selector 243 so that the queue selector 243 selects one of the output ports having the most ATM cells directed thereto.

This is different from the claimed invention of sequentially distributing input packets to a plurality of paths in an arrival order in units of packets.

It is respectfully submitted the Moriwaki is different from the claimed invention because Moriwaki reads from the queuing buffers based on the queue selector 243.

In contrast applicant claims sequentially distributing input packets to a plurality of paths in an arrival order.

Claims 12, 14-16 depend from claim 11 and include additional distinguishing features as pointed out above.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

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